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EXAMINER	
SMITH, FRANCIS P	

ART UNIT	PAPER NUMBER
1792	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,172	PARTRIDGE ET AL.	
	Examiner	**Art Unit**	
	Francis P. Smith	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 41-56* is/are pending in the application.

4a) Of the above claim(s) *31-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 41-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of invention I in the reply filed on August 7, 2008 is acknowledged.

2. Claims 31-40 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Response to Arguments

3. Claims 1, 10, 11, 22, 29, 41, and 50 are currently amended. Claim 56 is new. Claims 1-30 and 41-56 are currently pending and examined on the merits.

Regarding claim 16, Applicants' argue that one having ordinary skill in the art would not have formed and annealed silicon oxide on a substrate that includes a MEMS structure since such oxide layers tend to damage MEMS structures. The examiner notes that claim 16 does not require formation of a silicon oxide layer on a MEMS structure or even on the substrate. Therefore, applicant's arguments are apparently without merit. Furthermore, it was well known in the art at the time of the invention to form silicon oxide deposition layers overtop micromechanical chambers followed by annealing (see Reichenbach et al. (US 2004/0065932 A1, [0046] as evidence). In response to applicants' argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of

ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Addressing claim 27, Applicants' further argue that Yu/Polson/Torek as modified by Watanabe and Chen references does not teach or fairly suggest applying first and second etch residues and oxidizing the etch residue. The examiner respectfully disagrees. Watanabe teaches a two step etching process, which is analogous to first and second etching processes. Chen teaches ashing residue in oxygen gas in order to enhance the removal of said residue (see col. 1, lines 48-53). Therefore, one having ordinary skill in the art at the time of the invention would utilized Chen's residue oxidation process in Watanabe's etching method in order to remove the residue with the reasonable expectation of success.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-11 and 41-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Ito (US 6,436,790 B2).

Yu et al. teaches a method for forming a silicon oxide layer on a substrate. Regarding claims 1, 11, 41, and 51, a silicon oxide trench fill layer is formed through an ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method

employing tetra-ethyl-ortho-silicate (TEOS) as a silicon source material at an ozone:TEOS volume ratio of 13:1, a reactor chamber pressure of about 450 torr, and a substrate temperature of 620°C, which is analogous to positioning a substrate in a deposition chamber and oxidizing/decomposing a silicon precursor gas in a deposition chamber at a first temperature to form a silicon oxide layer (col. 9, lines 46-55). Then, the substrate was annealed at a second temperature of 1100°C, which is higher than the first temperature (col. 9, lines 25-35). Yu does not expressly disclose forming a silicon oxide layer via an iterative process.

Ito teaches a method for fabricating a semiconductor device in which a stress applied to each element formation region from each trench isolation region is sufficiently suppressed. Specifically, a first silicon oxide layer is formed (i.e. first sub-layer formed prior to all of the other of the sub-layers) followed by a heat/annealing treatment in order to place the film 6 in a thermally stable state (fig. 4c; col. 4, lines 49-65). A second silicon oxide layer 7 is then formed and heated/annealed (see fig. 4d; col. 5, lines 1-8). This multi-step film formation process is advantageous because the overall stress on the substrate is reduced to a level that will not affect substantial changes in electrical characteristics of the substrate (col. 5, lines 13-17). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to utilize Ito's repetitive oxide layer deposition in Yu's method in order to reduce the overall stress of the substrate.

As per claims 2 and 42, ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employed an oxygen (ozone carrier gas) flow rate of

about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60).

For claims 3,8,43, and 48, Yu discloses heating (annealing) the substrate in an oxygen-rich environment (col. 10, lines 49-55).

Regarding claims 4,9,44, and 49, Yu teaches a second temperature (1100°C) that is approximate to the highest processing temperature (about 920°C) col. 10, lines 4-12; col. 10, lines 49-55.

As for claims 5,6,45, and 46, a silicon layer was formed on a substrate at a low pressure of 10 T (col. 9, lines 36-45)

As per claims 7 and 47, ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employed an oxygen (ozone carrier gas) flow rate of about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60).

For claims 10 and 50, Yu employs a tetraethoxysilane (TEOS) as a silicon precursor gas (col. 9, lines 46-51).

6. Claims 12-15 and 52-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) and Ito (US 6,436,790 B2) as applied to claims 1 and 41, in view of Xia et al. (US 6,602,806).

7. Yu teaches a method for forming a silicon oxide layer on a substrate with the said substrate having an N or P-doping. Yu/Ito however is silent in respect to the silicon oxide layer containing a dopant.

Xia discloses a thermal CVD process for depositing a low dielectric constant carbon-doped silicon oxide film. Specifically, the method entails depositing a low dielectric constant film such as a carbon-doped silicon oxide layer deposited from a thermal CVD process (see abstract). Additionally, one or more dopants may be included with the organosilane and ozone during deposition of the low-k layer for both PMD and IMD applications. Phosphorus may be added using phosphine during the deposition described above to getter alkali metals (i.e. sodium), thereby reducing metal contamination of the deposited film. Boron may also be added using diborane. Alternatively, one or more dopants, such as phosphorus and/or boron, may be included in the process gas (col. 2, lines 66-67; col. 16, lines 58-68). Therefore, it would have been obvious to one skilled in the art at the time of the invention to utilize one or more dopants in the silicon oxide layer of Yu/Ito as taught by Xia to produce a film with a low dielectric constant for use in pre-metal and inter-metal dielectric layers to ultimately reduce the RC time delay of the interconnect metallization, to prevent cross-talk between the different levels of metallization, and to reduce device power consumption.

8. Claims 16-18,22-24,26, 29, and 30, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Polson et al. (US 6,544,898).

Regarding claim 16, Yu et al. teaches a method for forming a silicon oxide layer on a substrate. A silicon oxide trench fill layer is formed through an ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employing tetra-ethyl-ortho-silicate (TEOS) as a silicon source material at an ozone:TEOS volume ratio of

13:1, a reactor chamber pressure of about 450 torr, and a substrate temperature of 400°C (which is analogous to positioning a substrate in a deposition chamber (inherent) and oxidizing/decomposing a silicon precursor gas in a deposition chamber at a first temperature to form a silicon oxide layer) (col. 9, lines 46-55). Then, the substrate was annealed at a second temperature of 1100°C, which is higher than the first temperature (col. 10, lines 40-47). Yu, however, is silent with regard to forming a MEMS structure on a substrate.

Polson teaches a method of fabricating a MEMS device and teaches placing MEMS on semiconductor substrates (i.e. silicon wafers) (col. 1, lines 13-15). It would be obvious to one having ordinary skill in the art to add a MEMS device as taught by Polson to Yu's substrate in order to create micro electromechanical systems, such as high frequency circuits and MEMS accelerometers with the reasonable expectation of success.

For claim 17, Yu teaches an ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employed an oxygen (ozone carrier gas) flow rate of about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60).

As per claim 18, Yu discloses heating (annealing) the substrate in an oxygen-rich environment (col. 10, lines 49-55).

As for claims 22 and 26, Yu teaches a second temperature (1100°C) that is approximate to the highest processing temperature (about 920°C) col. 10, lines 4-12; col. 10, lines 49-55.

Regarding claim 23, Yu discloses a silicon layer was formed on a substrate at a low pressure of 10 T (col. 9, lines 36-45).

For claim 24, Yu teaches ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employed an oxygen (ozone carrier gas) flow rate of about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60).

For claim 29, Yu employs a tetraethoxysilane (TEOS) as a silicon precursor gas (col. 9, lines 46-51).

For claim 30, a silicon oxide layer formed through Yu's ozone assisted sub-atmospheric pressure chemical vapor deposition (SACVD) method yielded comparatively little shrinkage upon thermal annealing within an oxygen containing atmosphere, thus providing thermally oxidized contiguous layers where there is limited stress formed therein (col. 11, lines 16-25).

9. Claims 19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Polson et al. (US 6,544,898) as applied to claim 18 above, and further in view of Watanabe et al. (US 5,256,247).

Yu et al. as modified by Polson is silent with regard to etching the silicon oxide layer without producing an etch residue.

Watanabe teaches etching a chromium silicon dioxide layer of a resistor material in an electronic integrated circuit without the formation of etch residue (col. 7, lines 44-50). Therefore, it would have been obvious to one skilled in the art at the time of the

invention to adapt Yu's method as modified by Polson by incorporating Watanabe's etchant in order to prevent etch residue from hindering the performance of the integrated circuit.

Addressing claim 25, Yu discloses heating (annealing) the substrate in an oxygen-rich environment (col. 10, lines 49-55).

10. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Polson et al. (US 6,544,898), Watanabe et al. (US 5,256,247) as applied to claim 19 above, and further in view of Torek et al. (US 5,990,019).

Yu et al. as modified by Polson and Watanabe is silent with regard to etching the silicon oxide layer using a HF-vapor etch.

Torek et al. teaches a method of employing vapor phase etchants for etching oxides of silicon during the manufacture of a semiconductor devices that utilizes a gaseous mixture of HF and water as the etchant, which is analogous to a HF-vapor etch (col. 2, lines 46-54). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate Torek's HF-vapor etch in Yu's method as modified by Polson and Watanabe in order to remove native oxides and other types of oxide contaminants during capacitor formation without excessively attacking the doped silicon dioxide layer.

11. Claims 27, 28 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Polson et al. (US 6,544,898), Watanabe et al. (US 5,256,247), and Torek et al. (US 5,990,019) as applied to claim 21 above, and further in view of Chen et al. (US 5,904,570).

For claims 27 and 56, Watanabe discloses etching an oxide layer in two separate stages, which is analogous to applying a first and second etching process (col. 4, lines 4-10). However, Watanabe is silent regarding oxidizing the resulting residue.

Chen teaches a method for polymer removal after etching residue is exposed to an oxygen plasma, which is analogous to oxidizing etch residue (col. 2, lines 43-49). Therefore, it would be obvious to one skilled in the art at the time of the invention to adapt the method of Yu as modified by Watanabe, Polson, and Torek by further incorporating Chen's oxidizing plasma in order to effectively remove the etching residue to enhance subsequent manufacturing processes and ensure circuit functionality and reliability.

As per claim 28, Yu et al. as modified by Watanabe, Polson, and Torek is silent with regard to etching the silicon oxide layer using a HF-vapor etch.

Torek et al. teaches a method of employing vapor phase etchants for etching oxides of silicon during the manufacture of a semiconductor devices that utilizes a gaseous mixture of HF and water as the etchant, which is analogous to a HF-vapor etch (col. 2, lines 46-54). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate Torek's HF-vapor etch in Yu's method in order to remove native oxides and other types of oxide contaminants during capacitor formation

without excessively attacking the doped silicon dioxide layer.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Francis P. Smith whose telephone number is (571) 270-3717. The examiner can normally be reached on Monday through Thursday 7:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mikhail Kornakov can be reached on (571) 272-1303. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/F. P. S./
Examiner, Art Unit 1792

/Michael Kornakov/
Supervisory Patent Examiner, Art Unit 1792